WHAT IS CLAIMED IS:

1. A voltage conversion circuit, comprising:

a switch circuit arranged so that a series circuit constituted of a P-type transistor and an N-type transistor is provided between a pair of power source lines in series;

a smoothing circuit for smoothing an output voltage derived from a junction of the P-type transistor and the N-type transistor of the switch circuit;

a pulse signal generating circuit for generating one or more pulse signals, each of which has a duty ratio for obtaining a desired output voltage, by using the output voltage smoothed by the smoothing circuit as a power source, so as to give the pulse signal to a control terminal of the P-type transistor and a control terminal of the N-type transistor;

a start-up control signal for generating a control signal which forces the P-type transistor to turn ON and giving the control signal to the control terminal of the P-type transistor during a predetermined period on start-up.

2. The voltage conversion circuit as set forth in claim 1, wherein the start-up control circuit includes:

a start-up signal generating circuit for generating a start-up signal which has a predetermined voltage level

during the predetermined period on start-up; and

a switch control circuit, receiving the start-up signal and the pulse signal from the pulse signal generating circuit, which outputs a control signal whose voltage level causes the P-type transistor turn ON when the start-up signal has the predetermined voltage level, and outputs the pulse signal from the pulse signal generating circuit when the start-up signal does not have the predetermined voltage level.

3. The voltage conversion circuit as set forth in claim 1, wherein the pulse signal generating circuit includes:

a reference pulse signal generating circuit for generating a reference pulse signal in accordance with the output voltage from the smoothing circuit;

a delay circuit for delaying the reference pulse signal, which has been inputted, for the predetermined period; and

a delay time control circuit for setting a delay time of the delay circuit,

said voltage conversion circuit further comprising a step-up level shifter for increasing a voltage level of an output pulse signal of the delay circuit.

4. The voltage conversion circuit as set forth in claim

2, wherein the pulse signal generating circuit includes:

a reference pulse signal generating circuit for generating a reference pulse signal in accordance with the output voltage from the smoothing circuit;

a delay circuit for delaying the reference pulse signal, which has been inputted, for the predetermined period; and

a delay time control circuit for setting a delay time of the delay circuit,

said voltage conversion circuit further comprising a step-up level shifter for increasing a voltage level of an output pulse signal of the delay circuit.

5. The voltage conversion circuit as set forth in claim 1, wherein the start-up control circuit generates the control signal as a first control signal and also generates a second control signal for forcing the N-type transistor to turn OFF so as to give the second control signal to the control terminal of the N-type transistor during the predetermined period on start-up.

6. The voltage conversion circuit as set forth in claim 4, wherein the start-up control circuit includes:

a start-up signal generating circuit for generating a start-up signal having a predetermined voltage level

during the predetermined period on start-up;

a first switch control circuit, receiving the start-up signal and one of the pulse signals from the pulse signal generating circuit as a first pulse signal for the P-type transistor, which outputs a first control signal whose voltage level causes the P-type transistor turn ON when the start-up signal has the predetermined voltage level, and outputs the first pulse signal from the pulse signal generating circuit when the start-up signal does not have the predetermined voltage level; and

a second switch control circuit, receiving the start-up signal and another of the pulse signals from the pulse signal generating circuit as a second pulse signal for the N-type transistor, which outputs a second control signal whose voltage level causes the N-type transistor turn ON when the start-up signal has the predetermined voltage level, and outputs the second pulse signal from the pulse signal generating circuit when the start-up signal does not have the predetermined voltage level.

7. The voltage conversion circuit as set forth in claim 5, wherein the pulse signal generating circuit includes:

a reference pulse signal generating circuit for generating a reference pulse signal in accordance with the output voltage from the smoothing circuit;

a delay circuit for delaying the reference pulse signal, which has been inputted, for the predetermined period; and

a delay time control circuit for setting a delay time of the delay circuit,

said voltage conversion circuit further comprising:

a switch timing control circuit for generating the pulse signals as first and second pulse signals in accordance with an output pulse signal of the delay circuit;

a first step-up level shifter for increasing a voltage level of the first pulse signal from the switch timing control circuit; and

a second step-up level shifter for increasing a voltage level of the second pulse signal from the switch timing control circuit.

8. The voltage conversion circuit as set forth in claim 6, wherein the pulse signal generating circuit includes:

a reference pulse signal generating circuit for generating a reference pulse signal in accordance with the output voltage from the smoothing circuit;

a delay circuit for delaying the reference pulse signal, which has been inputted, for the predetermined period; and

a delay time control circuit for setting a delay time of the delay circuit,

said voltage conversion circuit further comprising:

a switch timing control circuit for generating the first and second pulse signals in accordance with an output pulse signal of the delay circuit;

a first step-up level shifter for increasing a voltage level of the first pulse signal from the switch timing control circuit; and

a second step-up level shifter for increasing a voltage level of the second pulse signal from the switch timing control circuit.

9. A semiconductor integrated circuit device, comprising a voltage conversion circuit including:

a switch circuit arranged so that a series circuit of a P-type transistor and an N-type transistor is provided in series between a pair of power source lines;

a smoothing circuit for smoothing an output voltage derived from a junction of the P-type transistor and the N-type transistor of the switch circuit;

a pulse signal generating circuit for generating one or more pulse signals, each of which has a duty ratio for obtaining a desired output voltage, by using the output voltage smoothed by the smoothing circuit as a power

source, so as to give the pulse signal to a control terminal of the P-type transistor and a control terminal of the N-type transistor; and

a start-up control signal for generating a control signal which forces the P-type transistor to turn ON and giving the control signal to the control terminal of the P-type transistor during a predetermined period on start-up.

10. The semiconductor integrated circuit device as set forth in claim 9, wherein the start-up control circuit includes:

a start-up signal generating circuit for generating a start-up signal which has a predetermined voltage level during the predetermined period on start-up; and

a switch control circuit, receiving the start-up signal and the pulse signal from the pulse signal generating circuit, which outputs a control signal whose voltage level causes the P-type transistor turn ON when the start-up signal has the predetermined voltage level, and outputs the pulse signal from the pulse signal generating circuit when the start-up signal does not have the predetermined voltage level.

11. The semiconductor integrated circuit device as

set forth in claim 9, wherein the pulse signal generating circuit includes:

a reference pulse signal generating circuit for generating a reference pulse signal in accordance with the output voltage from the smoothing circuit;

a delay circuit for delaying the reference pulse signal, which has been inputted, for the predetermined period; and

a delay time control circuit for setting a delay time of the delay circuit,

said voltage conversion circuit further comprising a step-up level shifter for increasing a voltage level of an output pulse signal of the delay circuit.

12. The semiconductor integrated circuit device as set forth in claim 10, wherein the pulse signal generating circuit includes:

a reference pulse signal generating circuit for generating a reference pulse signal in accordance with the output voltage from the smoothing circuit;

a delay circuit for delaying the reference pulse signal, which has been inputted, for the predetermined period; and

a delay time control circuit for setting a delay time of the delay circuit,

said voltage conversion circuit further comprising a step-up level shifter for increasing a voltage level of an output pulse signal of the delay circuit.

13. The semiconductor integrated circuit device as set forth in claim 9, wherein the start-up control circuit generates the control signal as a first control signal and also generates a second control signal for forcing the N-type transistor to turn OFF so as to give the second control signal to the control terminal of the N-type transistor during the predetermined period on start-up.

14. The semiconductor integrated circuit device as set forth in claim 13, wherein the pulse signal generating circuit includes:

a start-up signal generating circuit for generating a start-up signal having a predetermined voltage level during the predetermined period on start-up;

a first switch control circuit, receiving the start-up signal and one of the pulse signals from the pulse signal generating circuit as a first pulse signal for the P-type transistor, which outputs a first control signal whose voltage level causes the P-type transistor turn ON when the start-up signal has the predetermined voltage level, and outputs the first pulse signal from the pulse signal

generating circuit when the start-up signal does not have the predetermined voltage level; and

a second switch control circuit, receiving the start-up signal and another of the pulse signals from the pulse signal generating circuit as a second pulse signal for the N-type transistor, which outputs a second control signal whose voltage level causes the N-type transistor turn ON when the start-up signal has the predetermined voltage level, and outputs the second pulse signal from the pulse signal generating circuit when the start-up signal does not have the predetermined voltage level.

15. The semiconductor integrated circuit device as set forth in claim 13, wherein the pulse signal generating circuit includes:

a reference pulse signal generating circuit for generating a reference pulse signal in accordance with the output voltage from the smoothing circuit;

a delay circuit for delaying the reference pulse signal, which has been inputted, for the predetermined period; and

a delay time control circuit for setting a delay time of the delay circuit,

said voltage conversion circuit further comprising:

a switch timing control circuit for generating the

pulse signals as first and second pulse signals in accordance with an output pulse signal of the delay circuit;

a first step-up level shifter for increasing a voltage level of the first pulse signal from the switch timing control circuit; and

a second step-up level shifter for increasing a voltage level of the second pulse signal from the switch timing control circuit.

16. The semiconductor integrated circuit device as set forth in claim 14, wherein the pulse signal generating circuit includes:

a reference pulse signal generating circuit for generating a reference pulse signal in accordance with the output voltage from the smoothing circuit;

a delay circuit for delaying the reference pulse signal, which has been inputted, for the predetermined period; and

a delay time control circuit for setting a delay time of the delay circuit,

said voltage conversion circuit further comprising:

a switch timing control circuit for generating the first and second pulse signals in accordance with an output pulse signal of the delay circuit;

a first step-up level shifter for increasing a voltage level of the first pulse signal from the switch timing control circuit; and

a second step-up level shifter for increasing a voltage level of the second pulse signal from the switch timing control circuit.

17. The semiconductor integrated circuit device as set forth in claim 9, wherein the voltage conversion circuit is used as a step-down circuit for generating a driving voltage of the semiconductor integrated circuit device in accordance with an external power source voltage.

18. The semiconductor integrated circuit device as set forth in claim 13, wherein the voltage conversion circuit is used as a step-down circuit for generating a driving voltage of the semiconductor integrated circuit device in accordance with an external power source voltage.

19. A portable terminal, comprising the semiconductor integrated circuit device as set forth in claim 9.

20. A portable terminal, comprising the

semiconductor integrated circuit device as set forth in claim 13.